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Photovoltaic Manufacturing Technology - Phase I

Final Subcontract Report 9 January 1991 - 14 April 1991

S. Brown, D. S. Shen, and N. Heeke
Glasstech Solar, Inc.
Golden, Colorado



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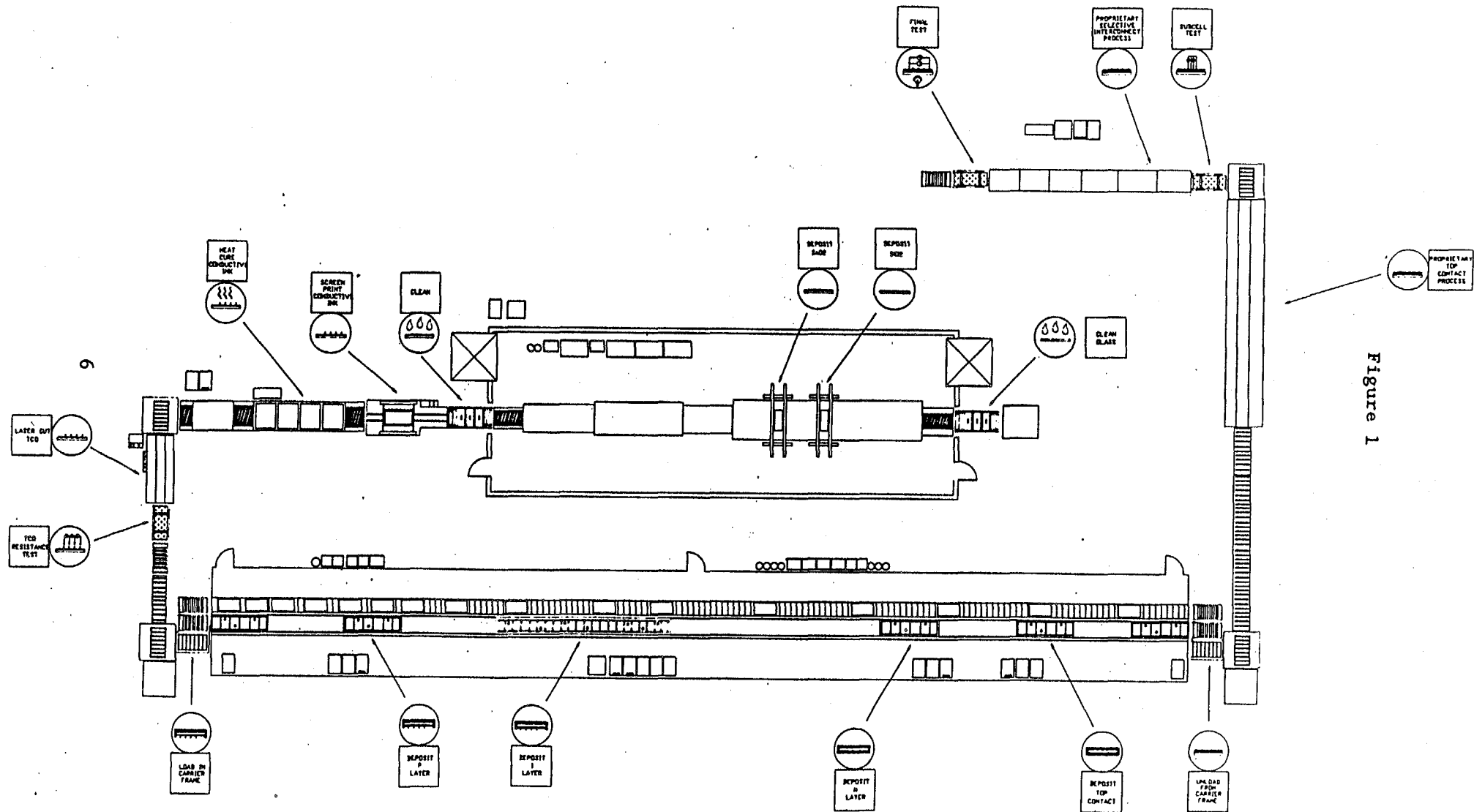
1.0 TASK I: DESCRIPTION

The current GSI manufacturing technology is based upon a continuous process photovoltaic production plant with a nominal annual capacity of 3.0 MW. The line is designed for a panel size of 40cm x 120cm and consists essentially of three sections:

1. The Front End, containing all processes (washing, TCO deposition, and patterning) needed to prepare the glass substrate for the PECVD process of depositing the amorphous silicon solar cell.
2. The P-I-N-M Section, in which the photovoltaic cell structure is deposited, including the back contact, without breaking vacuum.
3. The Back End, containing all processes (masking, etching, washing, subcell testing and repair, interconnection, and encapsulation) needed to complete the panel structure.

The plant design is highly flexible and can be configured for a variety of applications. The front and back sections include a number of rotate modules and spacer conveyors in addition to the process stations. These modules and conveyors give the line the ability to hold and release the glass panels according to the requirements of the process stations. All three sections are fully automated and computer controlled, and are operated asynchronously. Figure 1 shows the floorplan layout of the current manufacturing process.

Figure 1. Layout of Current Manufacturing Process



1.1 FRONT END SECTION

The front end process involves introduction of plain, beveled glass into the system, and the completion of the following steps:

- A. Initial Glass Cleaning
- B. Transparent Conductive Oxide Deposition
- C. Final Glass Cleaning
- D. Conductive Ink Screen Printing
- E. Ink Curing
- F. Laser Scribing
- G. Bus Bar/TCO Testing

1.1.1 Glass Cleaning

A Billco 150 Series flat glass washing and drying machine is used for the initial cleaning of the glass. The machine will handle any glass with smallest dimension of at least 7-3/4" up to a maximum width of 24" and a thickness range of 1/16" to 3". The process consists of five basic steps:

- a. Pre-spray Section
- b. Washing Section
- c. Rinse Section
- d. Final Rinse Section (DI Water)
- e. Drying Section

1.1.2 Transparent Conductive Oxide Deposition

The TCO Furnace is a major component of the photovoltaic processing system. Its purpose is to deposit a transparent, yet conductive, oxide (TCO) coating on a clear glass substrate. The coating is actually a two-layer film deposition consisting of silicon dioxide (SiO_2) and fluorine-doped tin oxide (SnO_2) layers. The SiO_2 layer is deposited first, on a clean glass

substrate, with a thickness of about 900Å. The second layer, fluorine-doped SnO_2 , is deposited on top of the SiO_2 layer with a thickness of about 6000Å. The method for these depositions is Atmospheric Pressure Chemical Vapor Deposition (APCVD).

1. To form SiO_2 layers on a glass substrate, the substrate is first heated to about 500°C; silane (SiH_4) and oxygen (O_2) are forced down onto the surface of the substrate. The SiO_2 layer prevents alkali diffusion from the soda-lime silicate glass, through the SnO_2 layer, to the device.
2. To form the layer of SnO_2 , the substrate is further heated to about 590°C. The SnO_2 layer is deposited from vapors of tin tetrachloride (SnCl_4) and water (H_2O) which are forced out of the SnO_2 injector. Additionally, hydrogen fluoride (HF) is supplied to provide fluorine as a dopant, and methanol (CH_3OH) is used to control the reaction rate.
3. The TCO Furnace consists of the following distinct sections:
 - a. Conveyor System
 - b. Heating Section
 - c. Process Injectors
 - d. Cooling System
 - e. Exhaust/ Scrubber System
 - f. Gas Manifold/ Bubbler System

1.1.3 Glass Cleaning

The $\text{SnO}_2\text{:F}$ layer deposited in the previous station is effectively a new, clean surface and as such is free from contaminants. However, loose particles of $\text{SnO}_2\text{:F}$ can often be present on the surface. These can easily be removed by a final cleaning station similar to the initial cleaning station. In this case, an enlarged heated drying blower is incorporated to completely remove residual moisture.

1.1.4 Conductive Ink Screen Printing

A high precision, high speed screen printer is used to print a bus bar and finger grid pattern on the TCO coated glass panel with a silver based ink. This pattern reduces the effective resistance of the TCO and is later used to form the solar panel.

1. The screen printer used is an Otto Isenschmid Corporation Model PC-GR-GS.
2. The machine is made up of the following major components:
 - a. Main Frame
 - b. Vacuum Equipment
 - c. Table Transport Belts
 - d. Squeegee, Flood, and Peel Off Mechanisms
 - e. Print Table
3. Technical Specifications
 - a. Maximum Print Area: 41cm x 121cm
 - b. Maximum Glass Size: 42cm x 122cm
 - c. Maximum Chase Size: 81cm x 172cm

1.1.5 Ink Curing

A Casso-Solar Corporation solar infrared furnace is used to cure the screen printed ink. It is a high temperature curing furnace (1600°F max. temp.) designed to ramp the glass temperature to 460°C, maintain this temperature for five minutes, and then start a gradual cooling of the glass. To achieve this, the Casso-Solar furnace curing section is divided into two heating and two cooling zones.

1. The first zone is intended to ramp the glass temperature to 460°C; to achieve this, a temperature setting of 650°C is used.
2. The second zone is intended to maintain glass temperature of 460°C \pm 10°C. To maintain this temperature, the second zone setting is 575°C.
3. The third zone is intended to gradually cool the glass; a temperature setting of 100°C is used.

4. In the fourth and last zone, a fully covered, unheated natural cooling zone will allow the glass temperature to be reduced to 120°C. Glass then exits the furnace.

1.1.6 Laser Scribing

The laser scriber uses an x-y table to move substrates under the focused beam of a Q switched YAG laser. TCO is removed to form electrically isolated rows for later series connection of the solar panel.

1. The pattern is stored in Superior Electric Company stepper motor indexers. Relative moves are used so that only the starting point needs to be changed to align the cut to the actual printed pattern. The starting point should only require adjustment if the laser is disturbed or the alignment of the screen printed bus bar/finger pattern changes. The final move will also require adjustment so that the table returns to home after the pattern is cut. Initial alignment is done empirically by cutting the pattern and measuring the offset. The table moves one inch for every 800 steps of the stepper motors.
2. When properly focused, the laser spot will have a diameter of approximately 150 μ m. Because of astigmatism in the optics, the beam will have an oval shape. The minimum minor diameter is approximately 70 μ m with a major diameter of 250 μ m. As the focusing lens is adjusted through the focal point, the minor axis shifts from the x axis to the y axis. This allows easy visual focusing by cutting crosses in TCO, which can be done using the manual jog buttons on the x-y table. The focus is adequate when there is no visually discernable difference in the widths of x and y cuts. With a new arc lamp, a current setting of 14-16 A and a frequency of 2.5-4 KHz will reliably cut TCO. As the bulb ages, the current will have to be increased to maintain the output power. Typical lifetimes for the arc lamps are 300-400 hours.

1.1.7 Bus Bar/TCO Testing

The tester is designed to test either 40cm x 40cm or 40cm x 120cm glass panels. The glass panels are precisely located by the centering conveyor. The test head is lowered to make contact with different points on the bus bar fingers and the TCO simultaneously. A microcomputer measures and stores the test values in memory. At the completion of the test, the test head is lifted up and the panel is advanced by the conveyor to the next position.

1. The bus bar test rejects a panel if any bus bar has a resistance $> 100\text{ K}\Omega$ or if 3 bus bar rows show a resistance $> 5\Omega$.
2. The TCO test rejects a panel if any two adjacent points have a resistance $> 20\Omega$ or if any point has a resistance $> 100\text{ K}\Omega$.
3. The scribe test rejects a panel if any line has a resistance $< 900\Omega$. It throws a warning flag if any line has a resistance $< 50\text{ K}\Omega$. It also tests the resistance between the first and last bus bar. If that reading is not $> 900\Omega$, the panel will be rejected. An operator will be called if there are 2 rejects within a group of 5 panels.

1.2 P-I-N-M SECTION

The P-I-N-M section is the key component of the photovoltaic production plant, capable of producing amorphous silicon solar cells at a rate of 1 MW/shift/year. Designed to handle glass substrates up to 40cm x 120cm (NEDO size), the system transports glass in a stainless steel carrier, for the purposes of uniform heating and grounding. This section deposits the P+, I, and N+ layers of a-Si:H which make up the photovoltaic cell and a silver layer which is used as the back contact.

1.2.1 PECVD Section

The P-I-N layers are deposited by means of Plasma Enhanced Chemical Vapor Deposition (PECVD). The glow discharge process involves flowing silane

gas at a controlled rate between two electrode plates, one grounded and the other carrying a radio-frequency (RF) potential. Within the RF field, a plasma is generated which decomposes the silane molecules, resulting in the deposition of silicon, as a thin film, onto a substrate being transported through the plasma.

- a. The P layer is boron-doped silicon carbide produced using a gas mixture of silane (SiH_4), methane (CH_4), and a boron dopant ($\text{B}(\text{CH}_3)_3$). The main requirements for the P layer are that it have a large bandgap to minimize absorption losses and a large conductivity to provide a large built-in field.

1. P process parameters

- a. Chamber Pressure 300-800 mT
- b. Substrate Temperature 120-200°C
- c. Total Gas Flow 50-450 sccm
- d. Layer Thickness 100-300Å
- e. RF Power 20-60 W

- b. The I layer is a straight amorphous silicon layer produced using only silane (SiH_4). The requirements for the intrinsic layer are that it have a low bandgap to absorb the light and a low density of states to allow complete collection of the generated carriers.

1. I process parameters

- a. Chamber Pressure 300-800 mT
- b. Substrate Temperature 150-220°C
- c. Total Gas Flow 400-1000 sccm
- d. Layer Thickness 2700-3500Å
- e. RF Power 100-250 W/ Electrode

- c. The N layer is phosphorus doped amorphous silicon produced using a gas mixture of silane (SiH_4) and phosphine (PH_3). The N layer requires a high conductivity so that a good Ohmic contact can be formed to the silver top contact.

1. N process parameters

- a. Chamber Pressure 300-800 mT
- b. Substrate Temperature 200-240°C
- c. Total Gas Flow 200-300 sccm

- d. Layer Thickness $\sim 300\text{\AA}$
- e. RF Power 75-150 W/ Electrode

1.2.2 Top Contact

Top contact metalization is achieved in line by direct current (DC) magnetron sputtering in GSI designed sputtering chambers. The chamber is set up with multiple rectangular cathodes to obtain the throughput which is needed.

- a. Metalization process parameters
 - 1. Chamber Pressure 2-8 mT
 - 2. Gas Flow 18-70 sccm
 - 3. Layer Thickness $\sim 5000\text{\AA}$
 - 4. DC Power 3.5 KW/ Cathode

1.3 Back End Section

The Back End process involves separation of the subcells and completion of the panel structure through the following steps:

- A. Maskant Screen Printing
- B. Chemical Etch
- C. Glass Cleaning
- D. Subcell Testing
- E. Selective Interconnect Screen Printing
- F. Ink Curing
- G. Full Panel Testing
- H. Encapsulation

1.3.1 Maskant Screen Printing

The screen printing machine is identical to the machine used on the front end. Amojell petrolatum snow white is screen printed as the mask. The mask pattern protects the silver back contact from being etched in the subcell areas.

1.3.2 Chemical Etch

The function of the etcher is to chemically remove excess sputtered silver back contact from the panel in order to isolate its cells. The etching process is conducted by subjecting the panel to a Ferric Nitrate ($\text{Fe}(\text{NO}_3)_3$) solution with a PH of one (1). The etching solution is set up in a recirculating system, and must be kept at room temperature for the best results.

1. The etcher is manufactured by Total Systems Concepts, Inc. and has the following distinct sections:
 - a. Etch Section
 - b. Rinse Section
 - c. Drying Section
 - d. Conveyor Mechanism
2. The etch time is approximately 30 seconds.

1.3.3 Glass Cleaning

The purpose of the glass cleaning station after the etcher is to remove the maskant material from the glass. As the glass enters the Total Systems Concepts, Inc. wash station, it is sprayed with a hot detergent solution to facilitate wetting of the glass surface. The glass panel then enters the scrubbing section through two hard rubber gate rollers. The scrubbing section contains two rollers which rotate at about 1700 RPM. The scrubbing section also sprays the glass panel with hot rinse water. The glass exits the scrubbing section through a set of chamois rollers which remove most of the water. After passing through the chamois rollers, a large heater/blower renders the glass completely dry.

1.3.4 Subcell Testing

The tester is designed to test either 40cm x 40cm or 40cm x 120cm glass panels. The glass panels are precisely located by the centering conveyor.

The test head is lowered to make contact with all 540 cells simultaneously. A microcomputer measures and stores the test values in memory to be used on the selective interconnect screen printer. The subcell test measures the current for a 0.6 V forward bias on each subcell. The test/mend/interconnect parameters are as follows:

- a. If $I < 1$ mA, then set interconnect file to print that subcell.
- b. If $I > 1$ mA, then try to mend the subcell and retest. The mending uses 4 V reverse bias with a 200 mS pulse.
- c. If I of retest > 20 mA, then set interconnect file to not print that subcell.
- d. If the number of bad subcells > 15 , then set the interconnect file to reject the entire panel.

1.3.5 Selective Interconnect Screen Printing

At the selective interconnect printer, the good cells are connected to the bus bar fingers to form the final series-parallel panel array. The printer uses the subcell information from the subcell test station to control 20 independent squeegees. Each squeegee prints a small pad of conductive ink which connects the back contact of a subcell to the nearest bus bar finger. This process allows us to better optimize the panel.

1.3.6 Ink Curing

A Casso-Solar Corporation solar infrared furnace is used to cure the interconnect ink. The furnace is similar to the furnace used on the front end.

1.3.7 Full Panel Testing

The Full Panel Tester is used to test the panel under AM1 illumination. The panel is precisely centered by the conveyor. The gantry is lowered to make contact with the two end, output bus bars of the array. The uniform AM1 illumination is generated by three 1000 W, M47 metal halide

bulbs. The bulbs are housed in a mirrored reflector enclosure. The output of the panel is measured under various load conditions. The results are compared by the computer to a set of standard values and a pass or fail signal is generated. Panels which test equal to or better than the standard values are released for final encapsulation and packaging.

1.3.8 Encapsulation

A Black Brothers Lamination Coater is used to apply Dymax Multi-Cure Coating as the encapsulant. The coating process is made by a film of sealant being carried on the coating roller and applied to the panel by pressure contact as the panel is drawn between this coating roller and the carrier rollers. An ideal coating would be a complete coverage of 2-5 mil of encapsulant. Thicker depositions are prone to be less resilient. Coating quality is controlled by pressure between the carrier and doctor rollers, as well as by pressure between the carrier roller and the panel. Following the application of encapsulant, the panel is carried by conveyor through an ultraviolet light chamber to cure the encapsulant. Three Fusion Systems, Inc. I300B ultraviolet light sources are used in the construction of this light chamber.

2.0 TASK II: POTENTIAL MODULE MANUFACTURING PROCESS CHANGES

Improvement in manufacturing costs and performance will require substantial changes in process and equipment configurations. The changes outlined below are explored in more detail in the following two sections.

2.1 PECVD Equipment Configuration

The throughput of an amorphous silicon production line is generally limited by the intrinsic layer deposition rate and the capital cost of the deposition equipment. We have found that the maximum effective deposition rate for i-layer material is approximately 6 Å/sec. Given this deposition rate barrier, the economics of the panel manufacturing process are determined by the equipment design and cost.

2.1.1 Vertical, Double-Sided Deposition Equipment

We believe that a vertically oriented PECVD system could be configured with a tandem transport design such that two panels could be processed in parallel as they pass through the deposition chambers. This system would nearly double the throughput of the PECVD system per capital dollar spent. Since the throughput rate for upstream and downstream equipment could be increased with little additional capital cost, the benefits would be substantial.

The equipment changes require a complete redesign of the transport system. Furthermore, a laminar flow of gases necessary for uniform film deposition may be more difficult to achieve in a vertical system. Therefore, the internal design will be modular and flexible so that electrode designs may be easily changed. The ability to test both a laminar cross flow design and a showerhead configuration will ensure the best electrode and gas delivery system for uniform gas depletion and deposition.

We propose separating the production line into three component segments. We believe that the maintenance requirements and run rates during the initial year or two of operation are sufficiently different between these segments to make continuous in-line production counterproductive. Furthermore, the cost of the glass handling equipment necessary for the loading of substrates onto vertical carriers is too high to justify any labor savings until the run rates have been optimized and tailored. The equipment could then be placed in an in-line configuration without significant additional cost or downtime.

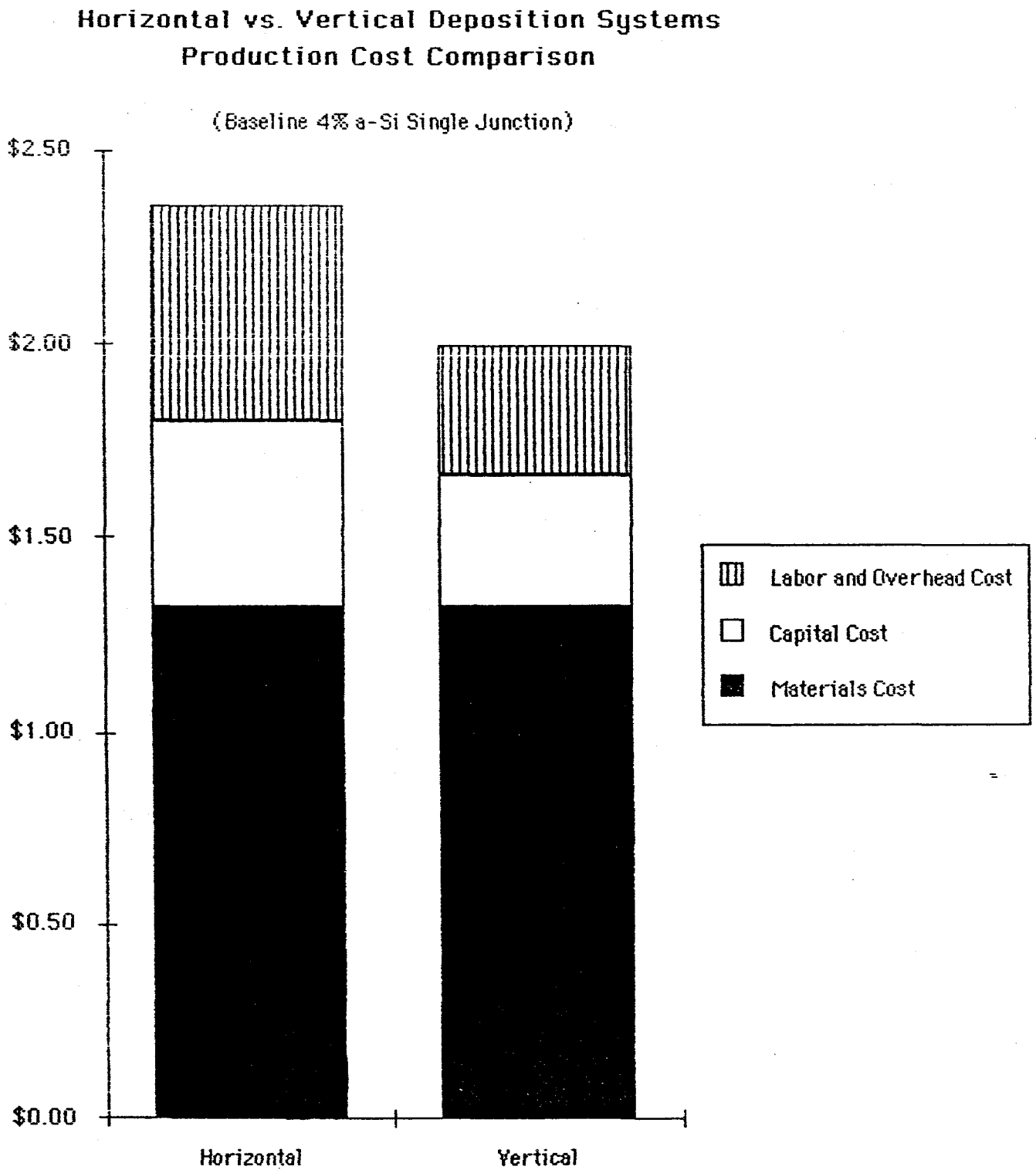
2.1.2 Cost and Performance Benefits

Figure 2 shows the cost benefit per watt of the additional throughput expected with the vertical configuration, assuming our baseline, single junction a-Si process. All the savings reflect reduced capital and labor cost per module produced. No savings have been assumed for consumables or utilities, although this is a conservative assumption since some purging gases and heating energy would be saved in the double-sided design.

The vertical design may yield additional benefits besides higher throughput. Companies designing vertical systems for sputtering and other vacuum applications report improved particulate counts on substrates. Although the GSI upward deposition design also produces limited quantities of particulates, the vertical design can yield the same results with less maintenance required. Particulate accumulates in catch basins well below the deposition area and outside the gas flow, requiring less frequent cleaning.

Transport systems for vertical chambers are also less expensive to operate and build. Glass sagging is not a problem, so larger substrates can be accommodated. Transports can be more easily shielded to further reduce particulate generation.

Figure 2. Cost Benefit From Vertical Throughput Configuration



2.2 Multijunction Modules

Multijunction amorphous silicon photovoltaic modules offer improved stability and efficiency when compared with single junction modules. Thin intrinsic layers suffer less degradation than the thicker layers of single junction cells, and variation of the band gaps of the intrinsic layer materials improves the collection efficiency of the modules. The combination of these two factors allows for a significant increase in stabilized module efficiency.

2.2.1 Multijunction Equipment Configuration

A manufacturing line for the production of multiple junction amorphous silicon photovoltaic modules requires additional vacuum chambers for the additional junction materials. The line configuration shown in Figure 3 is designed for the production of tandem junction modules. In a triple junction configuration, additional chambers are added for the extra junction. The process parameters and feed stock gasses vary for the different junctions, tailored to yield the most efficient set of material band gaps for energy collection. All front and back end processes, however, remain the same.

Note that using our modular chamber design, deposition chambers can be lengthened or shortened by adding or subtracting chamber modules. Depending on the choice of the bottom cell material, the first i-chamber could be short (e.g. for an a-Si/a-Si tandem, where the top cell is less than 70 nm) or long (e.g. for an a-Si/a-SiGe tandem, where the top cell could be 200 nm).

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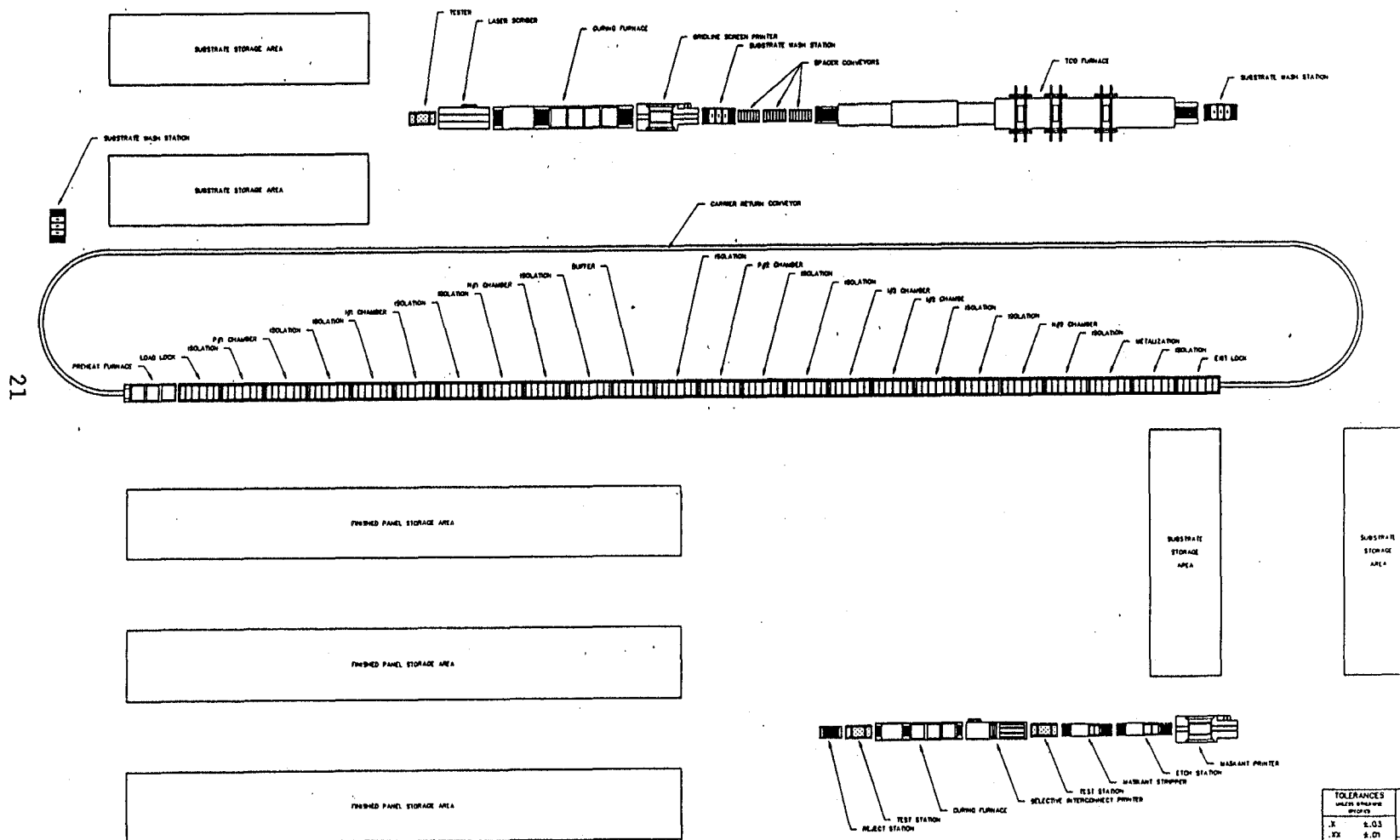


Figure 3

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2.2.2 Process Changes

2.2.2.1 Tunneling Junction

The tunneling junction is a key issue in fabricating amorphous silicon tandem solar panels. The tunneling junction must provide enough recombination centers so that any reverse-junction effect can be eliminated. Meanwhile, the junction should be transparent so that the optical loss can be reduced.

Currently there are two techniques for fabricating high quality tunneling junctions. One uses thin microcrystalline n- and/or p-layers in the tunneling junction. The other uses a thin layer of metal oxide (e.g., TiO_x or NbO_x) between the amorphous n- and p-layers.

Microcrystalline material is an ideal choice for the tunneling junction since it is transparent and conducting. The grain boundary states can provide recombination centers. However, it is difficult to deposit thin microcrystalline layers. The problem lies with the density of nucleation centers. Since the nucleation is not well controlled by deposition conditions and might be sensitive to the details of the system, thin microcrystalline layers may be difficult to deposit in a production line.

Tunneling junctions composed of a metal oxide between the amorphous n- and p-layers have properties similar to microcrystalline junctions. Currently we are using e-beam evaporated NbO_x in our research cells. NbO_x is conducting and transparent, so that a relatively thick layer (~10 nm) can be used. Thus, it can be easily sputtered on the panel in a large area production line. The GSI modular design allows easy insertion of an extra sputtering chamber between the n and p deposition chambers. In Figure 3, above, the tunneling junction is deposited in the chamber designated "buffer." More work is needed to study these tunneling junctions since, in the line, the metal oxide is coated on a hot substrate, whereas in our

research systems, the material has been coated on a cold substrate. Also, the properties of metal oxides may change with different deposition methods. Sputtered NbO_x may be somewhat different from e-beam evaporated NbO_x .

2.2.2.2 Bottom Cell Material

The advantage of an a-Si/a-Si tandem structure is that the material is relatively mature. GSI has carried out some intensive research on a-Si/a-Si tandem panels under a SERI subcontract. However, there are two disadvantages.

- The optical band gap of the material can be changed only in a very limited range. Without alloying, the band gap is adjusted through changing the hydrogen concentration. It is difficult to fabricate high quality low band gap devices. Thus the absorption spectrum of a-Si/a-Si tandem cells is basically the same as that of a-Si single junction cells. The only advantage of the a-Si/a-Si tandem is greater stability.
- The top cell is thin (~70 nm), and a small fluctuation in the thickness of the top cell will affect the current matching. Thus the demand for uniform deposition and thickness control is high.

An a-Si/a-SiGe tandem cell structure offers several advantages. By using a large portion of the solar spectrum, it is possible to develop high efficiency stable solar panels. Furthermore, many experimental data suggest that the a-SiGe alloy is more stable. However, there are also several disadvantages.

- Currently, most research groups have difficulty producing good quality low band gap SiGe alloys. The defect states are relatively high, and the efficiencies of the devices are relatively low. Furthermore, it is not clear that these materials are more stable than a-Si.

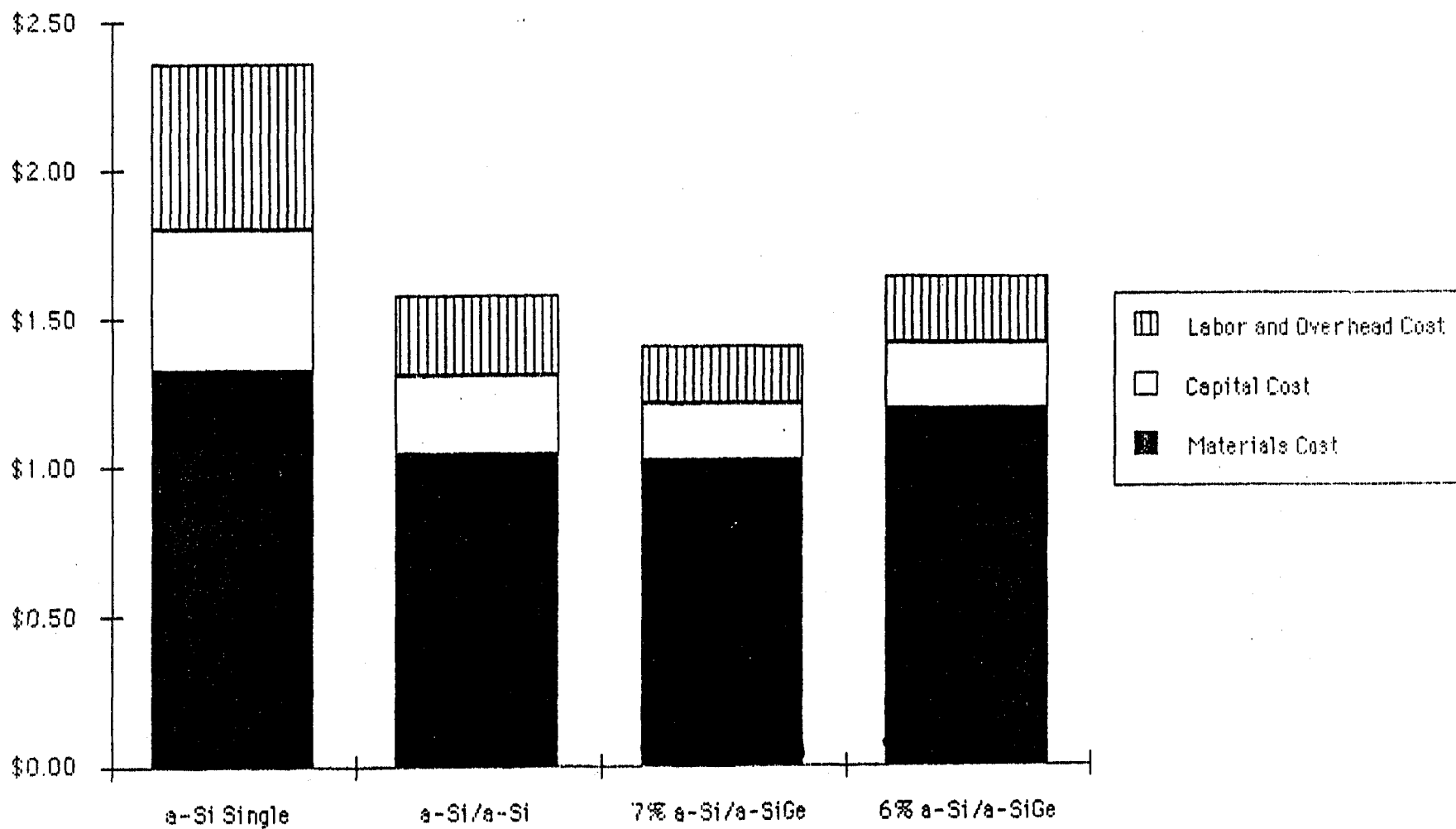
- There are two methods for fabricating high quality a-SiGe alloys. One uses SiH_4 (or Si_2H_6) and GeH_4 , heavily diluted in H_2 . The other uses a fluorinated source gas such as GeF_4 and SiF_4 . In either case, the growth rate for good material is low, a disadvantage in production.
- All state-of-the-art devices using a-SiGe alloys have incorporated band gap grading. The Ge concentration is changed near the interface as well as in the bulk. Since the a-SiGe intrinsic section of the tandem production line is long, and the dissociation rate of GeH_4 is high, grading is possible through control of the Ge source gas flow in different sections of the line.

Considering the above, we will base our production line modification on a-Si/a-SiGe tandems, experimenting with a-Si/a-Si panels, then adding Ge.

2.2.3 Expected Long Term Benefits

Although the capital equipment costs for multiple junction modules are higher than those for single junction modules, the improved stabilized efficiency justifies the additional cost. Figure 4 illustrates the production cost comparison between single junction and tandem junction modules. The single junction cost estimate is based on our baseline, horizontal process. The tandem junction estimates are based on vertical, high throughput systems. We believe that a reasonable assumption for the stable efficiency of a-Si single junction modules is 4.0%, while a similar assumption for a-Si/a-Si tandem modules is 5.0%. The high cost of germane greatly affects the cost of the a-Si/a-SiGe tandem modules. It is clear from the figure that, at a similar selling price per watt, using germane will be economically justifiable only if the efficiency of the modules exceeds 6.3%. We believe that it is reasonable to expect 7% stable efficiency a-Si/a-SiGe modules, but it is also true that the higher efficiency modules may command a price per watt premium in the market, since higher module efficiency means lower balance of systems costs.

Figure 4. Cost Comparison Between A-Si Single Junction, A-Si/A-Si Tandem Junction, and A-Si/A-SiGe Tandem Junction Modules



2.3 Improved Transparent Conducting Oxide (TCO), Semiconductor, and Back Reflector Processes

Various process changes can improve the efficiency of the modules. Each of the changes described has been shown in the laboratory to provide incremental improvement in cell efficiency. We believe that modifications in the in-line process can yield significant improvement in production module efficiency.

2.3.1 Multilayer TCO

High quality TCO is a critical element of high efficiency cells. As described in the previous section, the current GSI TCO is fluorine doped tin oxide ($\text{SnO}_2\text{:F}$), deposited in an APCVD process. Tin oxide, however, reduces in hydrogen, which is especially detrimental for $\mu\text{c-p}$ deposition where heavy hydrogen dilution is required. Furthermore, our current APCVD process produces a high haze TCO that is ideal for single junction amorphous silicon modules, but is not smooth enough for efficient nucleation and deposition of the precise semiconductor layers necessary for multijunction cells.

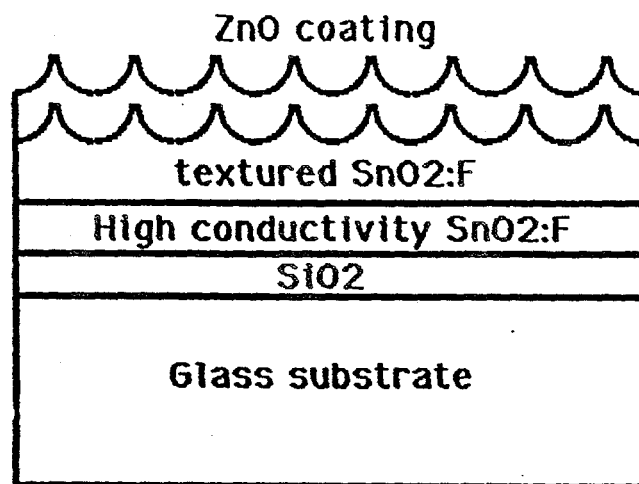
The surface morphology of the TCO should provide enough texture for light trapping and enough smoothness so that uniform thin p- and i-layers can be deposited. Using commercial TCO in lab cells, we have observed that the V_{oc} of the thin cells decreases with the cell thickness. The drop could be as high as 50 mV. A similar phenomenon has been observed by other research groups and has been corrected by using improved TCO morphology.¹

The surface morphology of the TCO can be changed by adjusting the gas flow ratio and deposition conditions in the TCO furnace. However, the conductivity and optical transmission of the TCO change at the same time. Furthermore, a compromise has to be reached between the transmission and the conductivity of the TCO. We propose a multi-layer TCO system. One

layer ($\text{SnO}_2\text{:F}$) would provide conductivity, a second layer ($\text{SnO}_2\text{:F}$) would provide morphology, and a third layer (ZnO) would provide protection from plasma. The total thickness of the TCO should not change much (to keep the transmission high), but the TCO furnace might need to be separated into sections. Figure 5 schematically shows the multi-layer TCO.

The concept of multi-layer TCO calls for a major change in the TCO furnace. However, the benefit could be substantial. The best a-Si/a-Si solar cell reported to date (10% stable efficiency reported by Fuji), used an improved TCO. The cell has both high V_{oc} (low V_{oc} drop for the thin top cell) and high current (better transmission).¹

Figure 5. Multilayer TCO Concept



2.3.2 μ C-P and/or Graded P-Layer

A μ c-p layer has been shown to substantially increase the V_{oc} of laboratory cells.² These layers can be formed by heavy hydrogen dilution of the film during deposition. Although the material is difficult to manufacture in a production environment on textured TCO, we believe that an improved TCO material, as described above, will allow the necessary changes in the process.

Graded p-layers can provide a necessary compromise between the conductivity and the band gap of the material. The conductivity and band gap of the p-layers are controlled by the carbon concentration in the film. When the carbon concentration is high, the band gap is high, the film is more transparent, and a high V_{oc} can be reached; however, the conductivity of the p-layer and the fill factor of the device are reduced. For a film with low carbon concentration, the conductivity is high but the band gap is low. In state-of-the-art lab devices, multi-layer (with different carbon concentrations in different layers) or graded carbon p-layers were used to achieve both high V_{oc} and good FF. In fact, in our lab cells, high carbon p-layers were used near the TCO/p interface and low carbon p-layers were used near the p/i interface. These cells have 11% efficiency. We expect that some of this increase can be transferred to large production modules.

2.3.3 Graded I-Layer

Two types of grading at the p/i interface have been shown to improve the performance of the solar cell: carbon grading and temperature grading.

Graded carbon interfaces have been used in our most advanced amorphous silicon solar cells, mainly for reducing the interface recombination. V_{oc} can be increased about 40 mV by using this interface layer. The carbon concentration in this layer is decreased from the p-layer to the i-layer.

Temperature grading of the i-layer also improves cell performance. We found that V_{oc} is affected by the band gap of the i-layer material near the p/i interface; that is, V_{oc} is higher for a higher band gap material near the p/i interface. Meanwhile, a lower band gap is preferred for the bulk i-layer, for improving the red absorption and stability. Temperature grading, therefore, can be used to achieve better efficiency. In fact, this technique has already been used in our small area lab cells. We expect it will be relatively easy to transfer these techniques to the production line with proper design changes.

2.3.4 Back Electrode and Patterning

The current GSI manufacturing process uses sputtered silver as a back contact and a mask/etch/wash process for patterning. Although this system has several advantages, including ease of pattern change, low capital cost, and the ability to selectively interconnect subcells, we have encountered severe problems with silver adhesion. Furthermore, we have found that the use of ITO as an interstitial layer between amorphous silicon and the metal can improve the J_{sc} .

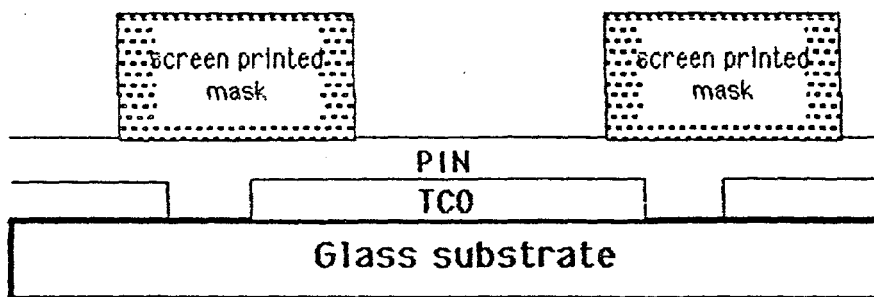
For our small area, thin, single junction (300 nm) lab cells, a 1 to 2 mA/cm² increase in J_{sc} was observed (compared with a pure Ag back reflector). The efficiency of the device can be raised about 15%. In a-Si/a-Si tandem cells, a similar increase was observed. Since the increase of the current is mainly in the red region of the spectrum, the current generated in the bottom cell is increased. This has the additional advantage of relaxing the demand on the top cell thickness control.

ITO can be sputtered in the metallization section of a production line. The thickness of the ITO should be about 100 nm. ITO/Ag or ITO/Ag/Al multi-layer back reflectors can be used. However, two problems have to be addressed: temperature and patterning. In our lab cells, ITO is sputtered when the cell is cool. In a production line, the panel is hot

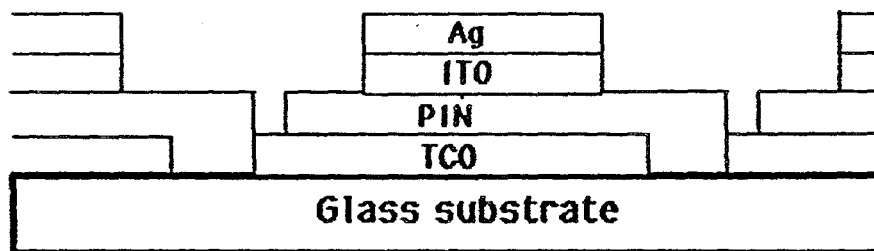
when it enters the metallization chamber. Whether this is beneficial or detrimental is not yet clear. Secondly, since the conductivity of ITO is high, it has to be patterned. Although ITO can be chemically etched, the etchant may affect the amorphous silicon. It may be possible to screen print a coating material on the separation lines of the subcells before ITO/Ag deposition, then clean the coating material, deposit blanket Al and laser scribe it. Although this requires removal of the panel from the vacuum chambers prior to the screen printing step, it is likely that a cooling step would be required before metallization in any case. The overall cost impact, therefore, would not be high. Figure 6 shows the back end metallization and patterning concept.

The new back contact calls for another major modification in the production line. But again, the modification may be justified by the benefit. A 15% increase in the efficiency is expected.

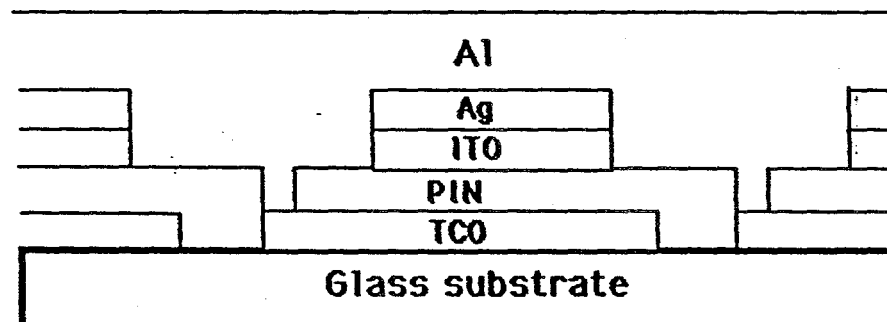
Figure 6. Back End Metallization and Patterning Concept



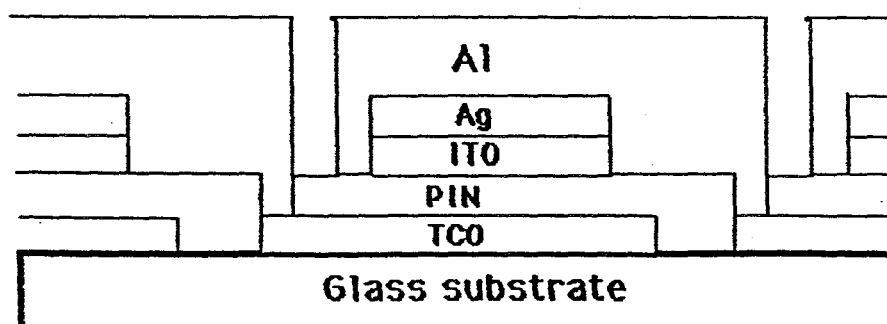
screen print mask
after pin
deposition



deposit ITO/Ag
wash off mask
laser scribe pin



Al deposition



laser scribe Al

2.3.5 Expected Benefits

The combination of the process changes described above should yield a substantial increase in module efficiency. Figure 7 shows the IV curve of a cell manufactured as part of a module produced on our baseline a-Si single junction production line. Figure 8 shows the IV curve of the entire module, demonstrating the expected efficiency drop between cell and module. Figure 9 shows the modeled QE and IV curves of the cells we expect to produce with the modified processes described above. Based on our experience, we expect a 15% drop between our modelled efficiency and the efficiency of the cells produced in a manufacturing process. We expect an additional 10-15% drop between cell efficiency and module efficiency, due to J_{sc} and FF losses as demonstrated by Figures 7 and 8. We expect a 5% area loss and a maximum 15% degradation loss. These calculations indicate a stable module efficiency exceeding 6.9%. We believe this is a conservative estimate.

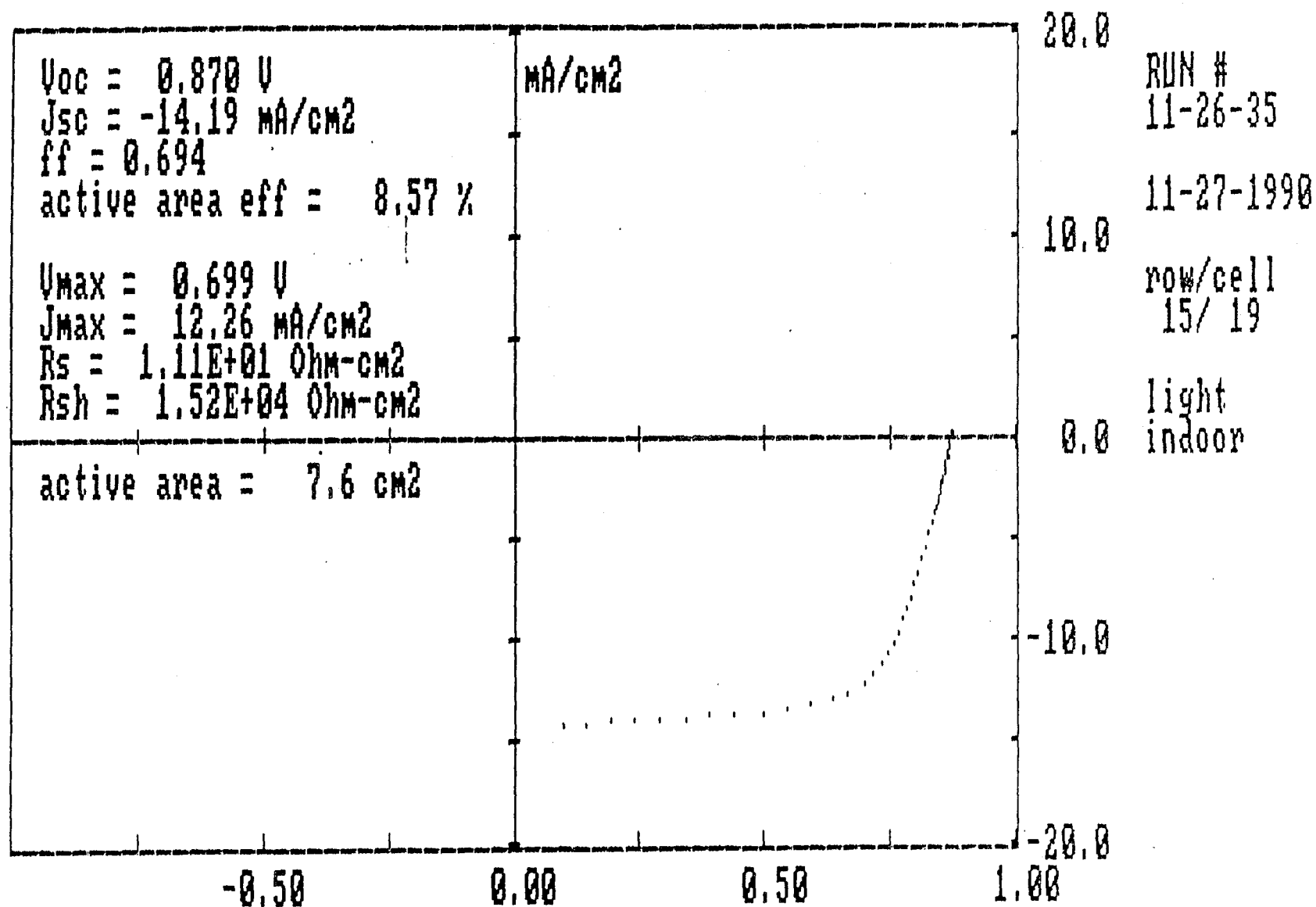


Figure 7. IV Curve of Current Process Cell

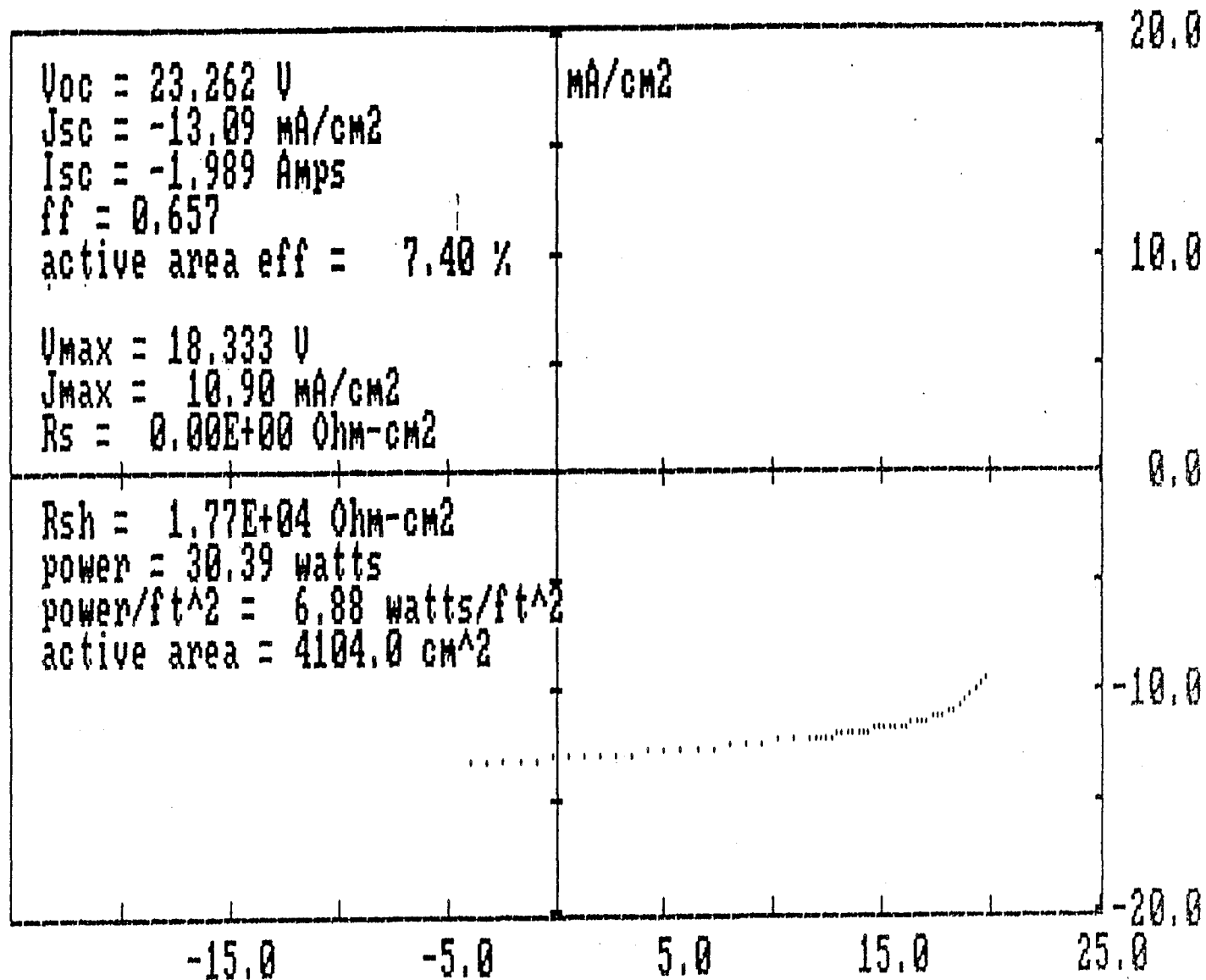
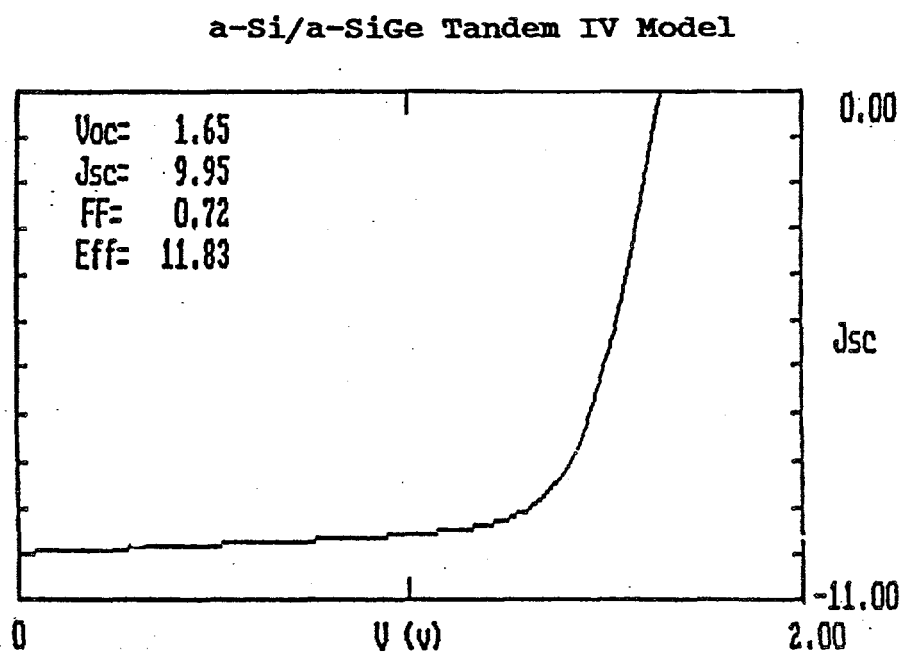
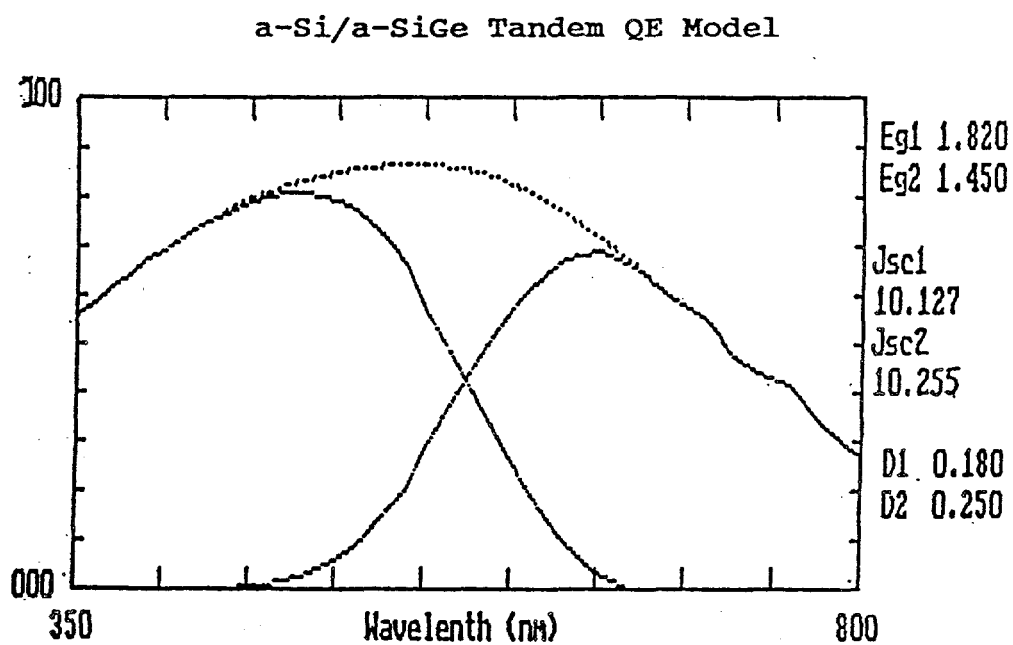


Figure 8. IV Curve of Current Process Module

Figure 9. QE and IV Curves of Concept Cells



3.0 TASK III: PROBLEMS ASSOCIATED WITH THE APPROACHES AND BENEFITS DESCRIBED IN TASK II

3.1 Potential Problems With Equipment Design

3.1.1 Uniform Gas Flow and Temperature Control

Uniform deposition of intrinsic and doped amorphous silicon layers over large areas is necessary to improve the performance of large area modules. This is especially true for multijunction modules since the layers are extremely thin, allowing little margin for error. A deviation in the thickness of the intrinsic layers in multijunction cells will cause locally unmatched currents and, therefore, severely reduce the subcell performance. Furthermore, the tunnel junction material must be thin enough to minimize absorption loss, but thick enough to provide efficient recombination. This optimization requires accurate thickness uniformity control.

Vertical reactors provide the obvious throughput advantages described above, but existing problems with gas flow and temperature uniformity need to be solved in the new design. In the current GSI horizontal reactors, nonuniform gas flow can cause particulate generation which would not be acceptable in multijunction processes. Furthermore, a vertical configuration may present new problems caused by the generally more severe temperature gradients in a vertical chamber. Film problems caused by non-uniform temperatures can be partially compensated through process parameter changes, but will also be addressed with a new heater design in the vertical system.

3.1.2 Transport Design

The current GSI horizontal configuration allows us to deposit upward onto an inverted module that has been inserted into a metal carrier that provides good ground contact. The current design yields panels with

relatively low particulate defect counts and uniform depositions, but some problems need to be solved. In the horizontal reactor, the transport mechanism is mounted directly to the electrode frame. During the deposition process, a-Si can form on the moving parts, causing mechanical failure and particulate generation near the film growth area.

The new vertical transport design should be well shielded so that moving parts above the deposition zone do not produce particle contamination. Furthermore, the transport design should provide an adequate back ground plane and TCO ground contact so that films will deposit uniformly.

3.2 Potential Problems With Multijunction Modules

3.2.1 Potential Problems With Multijunction Equipment Design

The design of equipment for multijunction modules presents no particular problems. Obviously, the number of chambers must be increased to allow for the deposition of the additional junction materials, but with GSI's modular equipment system, these additions are not difficult to design or implement.

3.2.2 Potential Problems With Multijunction Processes

3.2.2.1 Tunneling Junction

In our laboratory work, our metal oxide tunneling junction, NbO_x , has been deposited by evaporation. In the production line, the oxide would be sputtered in-line immediately after the top cell n-layer. Since the deposition process would be different, we would have to evaluate the material properties to make sure the sputtering process provides the desired results. Furthermore, the higher in-line deposition temperatures may cause changes in the material properties. In our laboratory cells, the NbO_x is deposited on a cold substrate.

3.2.2.2 Bottom Cell Material

As described in Task 2, there are several problems with both a-Si and a-SiGe as the top cell material. Aside from the difficulty of producing good low band gap material with a-Si material, the top cell of an a-Si/a-Si tandem must be quite thin, about 70 nm. For large production modules, maintaining good thickness uniformity in such a thin layer is difficult. Since even small variations in the thickness will affect the current matching, nonuniformity could be a serious problem.

An a-SiGe alloy allows a thicker top cell, eliminating the potential problems with thickness uniformity, but the material itself is difficult and slow to grow. The material will require careful process development and longer deposition times.

3.3 Potential Problems With Advanced Material Processes

3.3.1 Multilayer TCO

As described above, TCO is one of the key elements of high efficiency cells. A multilayer TCO allows for high conductivity, good surface morphology, and protection from plasma damage. This TCO structure, however, requires a specially designed deposition furnace capable of depositing the different layers with good process control. Furthermore, since the deposition conditions and temperatures will be different for the different layers, the furnace must maintain adequate isolation between deposition zones. Commercial furnaces are not capable of such functions, so a new design must be created. The GSI design described in Task 4 will be capable of four layer deposition.

3.3.2 μ C-P and Graded P-Layer

μ c-p layers can increase V_{oc} substantially, to > 0.9 V. However, it has been found that it is difficult to grow a thin μ c-p layer on textured TCO.

We think the problem lies with the density of nucleation centers. Even with heavy hydrogen dilution, the initial layer tends to be a mixture of amorphous and microcrystalline material. Without some thermal annealing, it appears difficult to produce good quality, crystalline phase material.

Our initial experiments with the deposition of a-Si:H,B and a-SiC:H,B films on TCO encountered problems during annealing. The films turned dark, then gradually transparent. We believe that the Si may react with SnO₂ during annealing, producing SiO₂ and Sn which may evaporate from the surface. In order to produce good μ c-p material, we believe that some protective layer may be necessary on the TCO to prevent such a reaction and allow the formation of good quality material. In Task 4, we describe a process which incorporates both thermal annealing and a protective layer over the TCO that should yield good results.

We have produced good laboratory results with graded p-layers. The production of a graded p-layer in a full scale manufacturing line, however, is more difficult since the substrates are in continuous motion and gas flows are more difficult to control precisely. Some isolation between gas flows of varying carbon concentration may be required so that the layers can be controlled precisely to achieve the needed grading.

3.3.3 Graded I-Layer

Grading the i-layer incurs problems similar to those encountered in grading the p-layer. Any grading, by either introducing carbon into an interface layer or varying the deposition temperature, requires careful process control during deposition.

The graded carbon layer may be deposited in the isolation chamber between the p- and i-chambers. Electrodes, gas lines and an RF power source are needed. A small amount of boron diffusion from the p-chamber is not important, since usually the graded carbon interface layer in our lab cells is deposited in the p-chamber. However, as in the case of graded p-layers,

separate electrodes and aero-dynamic barriers may be necessary.

Temperature grading should encounter few significant problems. The chambers and materials, however, will have to be designed to withstand the higher temperatures required for the low band gap material. Furthermore, since the temperature gradient will have to be controlled accurately for optimum results, separation between temperature zones and sophisticated temperature feedback controls may be needed.

3.3.4 Back Electrode and Patterning

The current method of applying a back contact through sputtering in-line immediately after the deposition of amorphous silicon limits the materials available for the back contact. Since the panels are hot at this point in the line, aluminum cannot be used. At high deposition temperatures, aluminum diffuses into the silicon. While silver does not diffuse, it is expensive and does not adhere well to the silicon.

Breaking the vacuum process adds capital expense initially, but with high throughput, the amortized expense does not add significantly to the manufacturing cost of the panels. Our proposed approach to the back contact and patterning steps, however, does present new challenges. A proper maskant must be found for use prior to ITO/Ag deposition, an effective double function etchant must be identified, the maskant should be easily cleaned, and the vacuum deposition chambers must be designed for economical operation. Our proposed design is described in Task 4.

4.0 TASK IV: GSI APPROACH FOR MANUFACTURING SOLUTIONS

4.1 PECVD Equipment Configuration

Although a vertical PECVD equipment configuration provides clear throughput advantages, the design of the gas delivery system, transport, and heater assemblies must account for the potential problems described in Task 3.

4.1.1 Uniform Gas Flow and Temperature Control

In the vertical reactor design, the gas inlet and exhaust plenums are mounted outside the electrode frame. This provides a straight, uniform gas flow across the electrode. Also, the plenums are designed for uniform flow at the inlet and exit plenum slits to reduce turbulence and provide a uniform gas source across the full length of the electrode. These designs should minimize particulate production in the deposition process.

In the current horizontal reactor design, multiple resistive heating elements are used to heat a thermal mass above the electrodes. The electrodes are not directly heated because of obstructions caused by the gas inlet and exhaust plenums. The heating elements are connected to a circuit inside the vacuum chamber, which, at certain temperatures and pressures, can cause arcing and element failure.

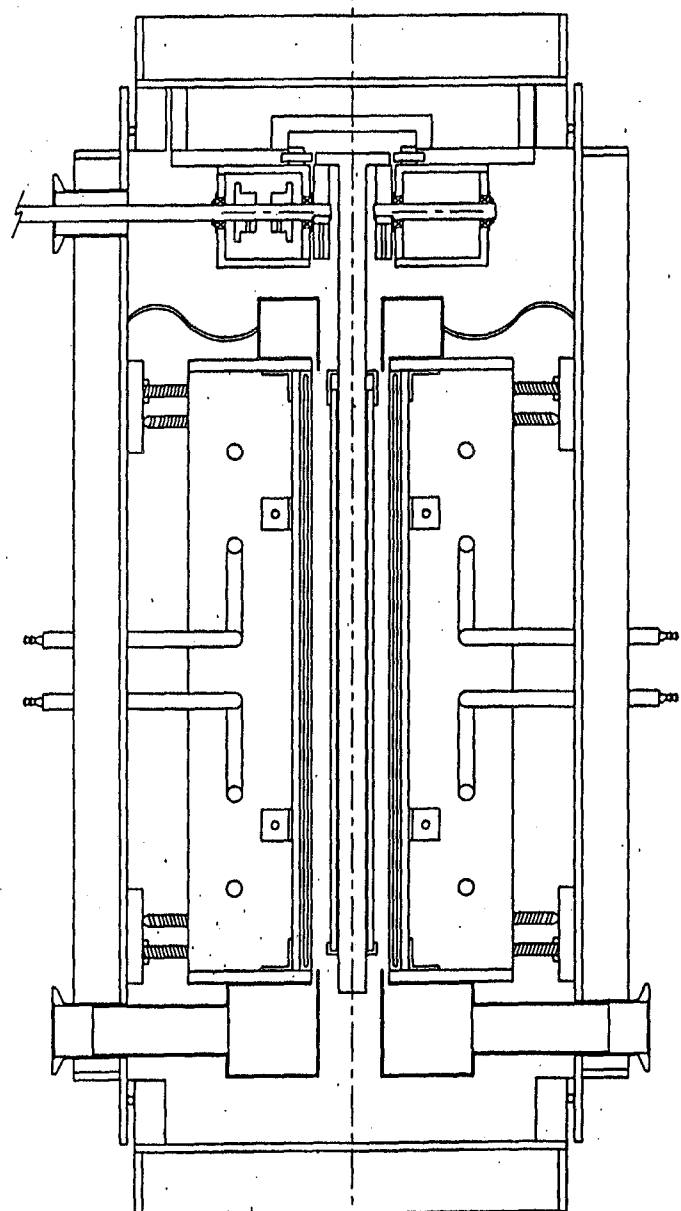
In the vertical reactor design, a single, formed resistive heating element is designed such that all electrical connections are made outside of the vacuum chamber. With the removal of the plenums from under the electrode frame, the element is placed directly behind the electrode surface to provide the film growth area with much more uniform temperatures. Also, a thicker electrode backing plate has been designed to provide a larger heat mass and disperse the heat more uniformly across the electrode.

4.1.2 Transport Design

In the current horizontal reactor, the transport mechanism is mounted directly to the electrode frame, causing deposition on the transport and particulate generation. In the vertical design, the transport mechanism has been moved out of the deposition zone, reducing the amount of a-Si that can reach the moving components. This should dramatically reduce maintenance cost, improve uptime yields, and improve film quality. Shields will trap any particulate generated by the moving parts. Contact brushes on the lower edge will provide good TCO ground contact for improved uniformity.

Figure 10 illustrates the internal transport and chamber design concept for the vertical, double-sided reactor. All of the components have been designed in a modular form to allow easy retrofitting of new components, including showerhead gas delivery systems if these demonstrate better performance.

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Figure 10. Internal Design Concept for the Vertical, Double-Sided Reactor

4.2 Multijunction Modules

4.2.1 Multijunction Equipment Design

As explained above, the GSI modular design allows relatively easy insertion of additional deposition modules into the PECVD line for additional junction materials. Figure 3, above, illustrates the design concept.

4.2.2 Multijunction Process Proposals

4.2.2.1 Tunneling Junction

Our initial analysis indicates that sputtered NbO_x should perform as well as e-beam evaporated material as a tunneling junction, although a slightly thicker layer may be necessary. The layout in Figure 3, above, shows the line with a tunneling junction sputtering chamber (buffer chamber) between the top cell n-layer and the bottom cell p-layer. If high temperature deposition causes problems, additional cooling sections of the line may be added, but we do not anticipate such problems.

4.2.2.2 Bottom Cell Material

Since the thickness uniformity problems associated with a-Si/a-Si solar cells are likely to be severe in a production environment, we expect to design the equipment for a-Si/a-SiGe modules. The a-SiGe i-layer deposition section will incorporate air flow isolation curtains to facilitate the Ge grading necessary for high quality low band gap material. The modular nature of GSI equipment facilitates this design; all chambers will be of uniform length with air flow curtains between the first several chambers for good quality grading.

Since the deposition rate of high quality a-SiGe material is low, the bottom cell i-layer deposition section must be long to maintain high

throughput. Again, the modular system allows easy extension of the design. The configuration described in Figure 3, above, can be easily adjusted to match the required deposition rate.

4.3 Advanced Material Processes

4.3.1 Multilayer TCO

The concept for multilayered TCO is described in Task 2. As described in Task 3, the multilayer process requires a unique APCVD furnace design. Our APCVD system, developed in conjunction with Asahi Glass Company, Japan, includes multiple injectors for multilayered coatings. In our current process, the layers include only SiO_x and $\text{SnO}_2:\text{F}$. With an extension of the furnace, however, we believe we can easily accommodate an additional SnO_2 layer for better surface morphology, and a ZnO layer for protection.

The furnace will require good temperature isolation and control between layers. In our current concept, air curtains and insulation layers help to isolate multiple heating and cooling zones that allow precise temperature control. Figure 11 illustrates the design.

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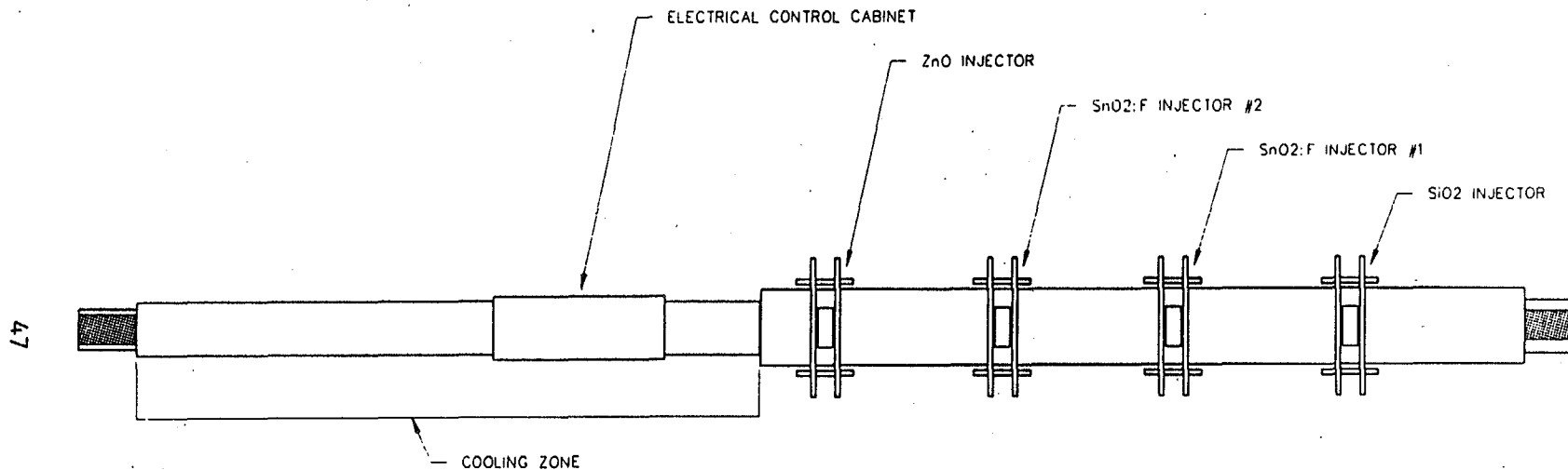


Figure 11. Multilayer TCO APCVD Furnace Design Concept

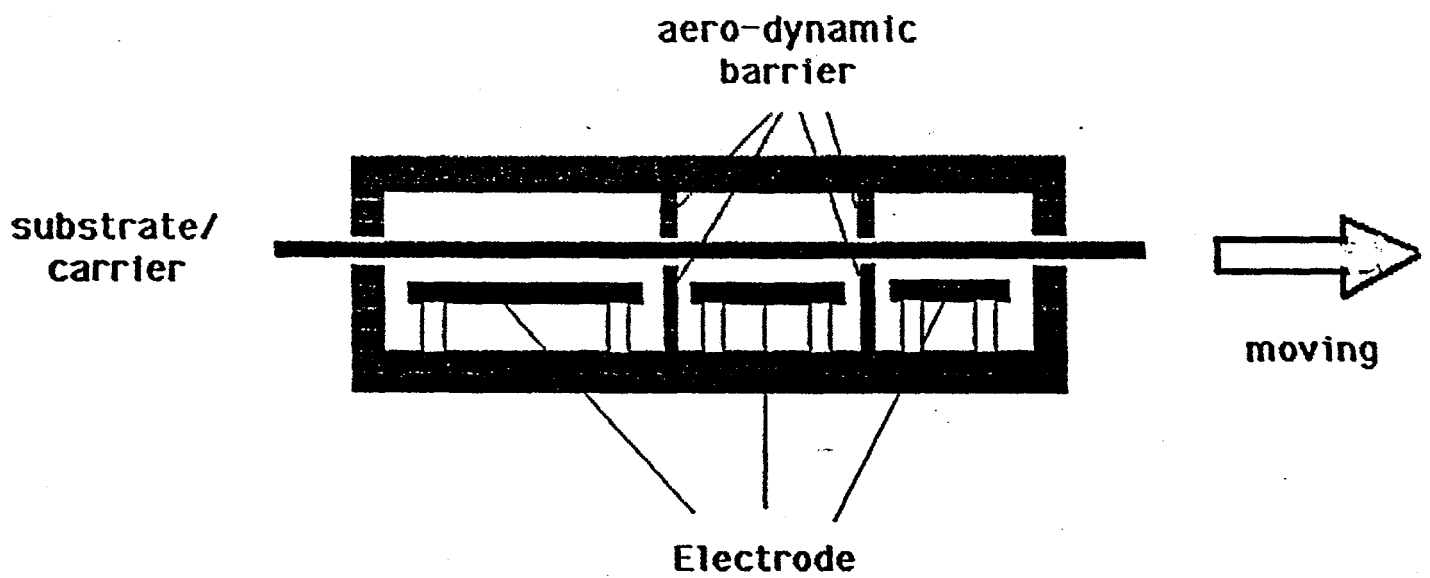
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FRACTIONAL	±1/16	DESIGNED	DATE	GS1/SERI MANUFACTURING INITIATIVE MULTI-LAYER TCO, FURNACE LAYOUT, CONCEPT DRAWING	
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4.3.2 μ C-P and Graded P-Layers

Based on preliminary results, we believe in-situ rapid thermal annealing of a thin a-Si p-layer may be an effective way of creating a μ c-p-layer. In a production line, this means that a rapid thermal annealing system will be assembled in the isolation chamber between the p-and i-chambers.

In a production line, depositing a graded p-layer requires control of the CH_4 concentration in the chamber. A high CH_4 concentration is preferred near the entry-port and a low CH_4 concentration is preferred near the p/iso-chamber. Since the p-chamber is short and gas mixes very quickly, just injecting CH_4 near the entry-port is not enough. It is not necessary, however, to completely isolate the p-chamber into different sections. A multi-electrode design with aero-dynamic barriers should provide adequate isolation for the grading process. Figure 12 illustrates the idea.

Figure 12. Chamber Configuration Concept for Graded P- and I-Layers



4.3.3 Graded I-Layer

The i-layer grading will require design changes similar to those described above for p-layer grading. A multi-electrode configuration with air curtain barriers will allow CH_4 grading at the interface. In addition, the temperature will have to be precisely controlled during the deposition process. This requires not only separate heater zones that can rapidly change the substrate temperature, but also in-situ thermocouples that will provide temperature feedback for the computer control system. The vertical chamber design includes proximity thermocouples that accurately measure the substrate temperature without disrupting the deposition process.

4.3.4 Back Electrode and Patterning

Currently, we are using Ag as a back contact/reflector. As described above, however, Ag has a severe adhesion problem. On the other hand, Al has good adhesion, but has a diffusion problem (into n^+) and its reflectivity is lower than that of Ag. We tested a ZnO (undoped)/Al structure and achieved good results. ZnO acted as a diffusion barrier. In fact, after weather testing and thermal cycling, the FF of the device improved (we speculate that Al doped the ZnO). However, since the ZnO is undoped, this layer has to be very thin (~1 nm). In a production line, it is difficult to deposit such a thin layer over large areas. Thus a doped ZnO or ITO is preferred.

Our proposed solution includes in-line deposition of sputtered ITO, screen printing, Ag sputtering, maskant cleaning, Al sputtering, and laser scribing. The process should produce a back contact with excellent conductivity and reflectivity. The Al should provide an adhesive protective layer over the Ag. And, the laser scribing process will eliminate the need for front grid lines and produce a module with very low area loss. Figure 13 illustrates the back end process steps and equipment configuration needed.

Note that additional equipment needed in the back end process is offset by equipment no longer needed in the front end process (i.e. grid line screen printer, curing furnace, laser scribe, and tester).

Several maskant materials used in the semiconductor industry have been investigated for possible use after deposition of the ITO. Some of these materials may require a photocuring step prior to Ag sputtering. This process step is easy to incorporate into the line.

5.0 CONCLUSION

The ideal future tandem amorphous silicon solar module using a glass substrate will have the following structure:

- glass
- TCO (multi-layers of SnO_2 and ZnO)
- p ($\mu\text{c-p}$; multi-layer or graded carbon a-SiC:H,B)
- Graded interface layer (a-SiC:H and/or temperature grading)
- i_1 (a-Si:H)
- n (a-Si:H,P)
- Metal oxide (not necessary if thin $\mu\text{c-n}$ layer can be fabricated)
- p ($\mu\text{c-p}$ or a-SiC:H,B)
- i_2 (a-Si:H or a-SiGe)
- n (a-Si:H,P)
- Back reflector (e.g., ITO/Ag/Al)
- Encapsulation (e.g., SiO_2 , SiN and/or polymer; or glass-glass)

The stable efficiency of today's amorphous silicon "state-of-the-art" lab cells is around 8%. Cells with 10% stable efficiency have been reported, but in the field, efficiency as low as 2-3% is common. Obviously, new production processes are necessary.

GSI has more equipment design experience than any other manufacturer of amorphous silicon deposition equipment, and is the only company in the United States dedicated to the manufacturing equipment market. We believe the concepts described above represent the best designs for improved thin film module production. Since the technology is still developing, a future production line should include enough flexibility to allow the incorporation of new technologies. The GSI design allows relatively easy modification of the production process.

References

1. Y. Ichikawa, S. Fujikake, T. Yoshida, T. Hama, and H. Sakai, Proceedings of the 21st IEEE Photovoltaic Specialists Conference, Kissimee, Florida (1990), p. 1475.
2. P. Bhat, S. Brown, R. Hollingsworth, D.S. Shen, et. al., "Research on Stable, High Efficiency Amorphous Silicon Multijunction Modules," Phase I Semi-Annual Progress Report for SERI Subcontract No. ZM-0-19033-3, March 1991, p. 46.

Appendix 1: Summary Per Watt Cost Comparison
a-Si, a-Si/a-Si, and a-Si/a-SiGe Modules

Assumptions:

- 7 year depreciation on equipment
- 30 year depreciation on building
- stable conversion efficiency = 4% for a-Si, 5% for a-Si/a-Si, and 6% or 7% for a-Si/a-SiGe
- annual production capacity for 2 shifts = 90,000 panels for single, 180,000 for tandem
- panel size = 2 ft. x 4 ft.

	a-Si Single	a-Si/a-Si	7% a-Si/a-SiGe	6% a-Si/a-SiGe
Materials Cost	\$1.32	\$1.04	\$1.02	\$1.19
Capital Cost	\$0.48	\$0.27	\$0.19	\$0.23
Labor and Overhead Cost	\$0.56	\$0.27	\$0.19	\$0.22
TOTAL	\$2.36	\$1.58	\$1.40	\$1.64

Appendix 2: Production Cost Estimate Detail
Comparison of a-Si, a-Si/a-Si, and a-Si/a-Si Modules

Assumptions

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1. Steady state operation after three years breakin.
2. A-Si single junction modules use baseline process.
3. New TCO and back contact used in both tandem modules.
4. Additional electricity and maintenance costs required for high throughput tandem module production.

	a-Si Single \$/sq. ft.	a-Si/a-Si \$/sq. ft.	a-Si/a-SiGe \$/sq. ft.
MATERIALS			
1/8" seamed glass (precut)	\$0.85	\$0.85	\$0.85
Tin oxide process gases			
Silane	\$0.10	\$0.10	\$0.10
SnCl ₄	\$0.01	\$0.01	\$0.01
HF	\$0.10	\$0.15	\$0.15
O ₂	\$0.19	\$0.25	\$0.25
Zn source gas	\$0.00	\$0.15	\$0.15
Washing detergent	\$0.00	\$0.00	\$0.00
Deionized water	\$0.04	\$0.04	\$0.04
PIN process gases			
Silane	\$0.70	\$0.95	\$0.95
Trimethylboron	\$0.06	\$0.13	\$0.13
Phosphine	\$0.07	\$0.14	\$0.14
Germane	\$0.00	\$0.00	\$1.95
Methane	\$0.01	\$0.02	\$0.02
Argon	\$0.02	\$0.03	\$0.03
Hydrogen	\$0.01	\$0.01	\$0.01
Nitrogen	\$0.02	\$0.03	\$0.03
SF ₆	\$0.01	\$0.02	\$0.02
Sputtering targets	\$0.45	\$0.90	\$0.90
Screen print ink	\$1.70	\$0.00	\$0.00
Maskant	\$0.02	\$0.30	\$0.30
Stripper	\$0.00	\$0.10	\$0.10
Screens	\$0.01	\$0.01	\$0.01
UV encapsulant	\$0.20	\$0.20	\$0.20
Packaging	\$0.40	\$0.40	\$0.40
Subtotal	\$4.96	\$4.78	\$6.73

<u>Utilities</u>			
Electricity	\$0.20	\$0.22	\$0.22
Water	\$0.05	\$0.05	\$0.05
Gas	\$0.01	\$0.01	\$0.01
Subtotal	\$0.26	\$0.28	\$0.28
<u>Maintenance</u>			
Pump rebuild	\$0.03	\$0.05	\$0.05
Pump oil	\$0.03	\$0.05	\$0.05
Filters	\$0.01	\$0.02	\$0.02
Subtotal	\$0.07	\$0.12	\$0.12
TOTAL	\$5.29	\$5.18	\$7.13

Production Cost Estimate (cont.)

<u>Capital Cost Estimate</u>	<u>a-Si</u>	<u>a-Si/a-Si</u>	<u>a-Si/a-SiGe</u>
Equipment Cost	\$9,000,000	\$13,000,000	\$13,000,000
Building Cost	\$3,010,000	\$3,010,000	\$3,010,000
TOTAL	\$12,010,000	\$16,010,000	\$16,010,000

Labor & Overhead Cost Estimate

- increase for tandems necessary to handle higher throughput

	<u>Single Junction</u>		<u>Tandem</u>	
	<u>Number</u>	<u>Cost</u>	<u>Number</u>	<u>Cost</u>
Direct Labor	30	\$750,000	35	\$875,000
Maintenance and Support	10	\$250,000	15	\$375,000
Administrative	10	\$400,000	12	\$480,000
Non-labor Overhead	0	\$200,000	0	\$200,000
TOTALS	50	\$1,600,000	62	\$1,930,000

Appendix 3: Per Watt Cost Analysis for a-Si/a-SiGe Modules
Variable Efficiency and Yield Parameters

Assumptions:

- 7 year depreciation on equipment
- 30 year depreciation on building
- conversion efficiency presumed stable (post-degradation)
- production capacity for 2 shifts = 180,000 panels per year
- panel size = 2 ft. x 4 ft.

Efficiency(%)	6%	7%	8%	9%
Materials Cost	\$1.19	\$1.02	\$0.89	\$0.79
Capital Cost	\$0.23	\$0.19	\$0.17	\$0.15
Labor and Overhead Cost	\$0.22	\$0.19	\$0.17	\$0.15
TOTAL	\$1.64	\$1.40	\$1.23	\$1.09
Yield Adjustment				
70%	\$2.34	\$2.01	\$1.76	\$1.56
80%	\$2.05	\$1.76	\$1.54	\$1.37
90%	\$1.82	\$1.56	\$1.37	\$1.21
100%	\$1.64	\$1.40	\$1.23	\$1.09

Appendix 4: Vertical vs. Horizontal Deposition Systems
Per Watt Production Cost Comparison

(Baseline a-Si single junction, 4.0% efficiency)

	Horizontal	Vertical
Materials Cost	\$1.32	\$1.32
Capital Cost	\$0.48	\$0.34
Labor and Overhead Cost	\$0.56	\$0.34
TOTAL	\$2.36	\$2.00

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16. Abstract (Limit: 200 words) This report describes the Glasstech Solar design concepts for improved thin-film module production, including three process steps: (1) The front-end step includes washing, transparent conductive oxide (TCO) deposition, and patterning. (2) The P-I-N-M step is that in which the photovoltaic cell structure is deposited, including the back contact, without breaking vacuum. (3) The back end step includes masking, etching, washing, subcell testing and repair, interconnection, and encapsulation. The design is flexible and can be configured to a variety of applications. The front and back sections (steps 1 and 3) include a number of rotate modules and spacer conveyors. These modules and conveyors enable the line to hold and release glass panels according to the requirements of the process stations.			
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